**CPU Design Project- Part 6**

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* **What did you learn from this project?**

The CPU design project make us have a better understanding of the architecture and operation of CPU. We use multi-cycle to design the CPU. The software tool is ModelSim, Altera Quartus II IDE. During the project makes us get more familiar with the VHDL coding and debugging. In the project, the ISA helps us know about what the order could be implemented by the digital codes, among the individual components (registers, multiplexers, control unit, datapath) of the CPU, we learned the importance of the cycle of the computer. It is required strictly to make each cycle work normally. Moreover, we build the memory to store and load the data. The simulation by Modelsim help us observe the data correspondingly to the clock, reset, a control signal. Combine datapath and memory on the FPGA together, and it gives us a more practical understanding of this design.

* **What would you do differently next time?**

Next time, I think that I could try different methods of designing CPU. Since this time I use the multi-cycle. Next time, we will try pipeline datapath. Different methods of designing the CPU may have quite different ways to consider the clock cycle, delay, etc. So trying different method could help us have different perspectives of the CPU design. After then, we could compare the advantages and disadvantages of them.

* **What is your advice to someone who is going to work on a similar project?**

Firstly, I think we will recommend the future students take into account every details in their design, even very small error or ignorance may result in long time confusion. Moreover, read more related books, journals, only a solid knowledge background can increase the ability to solve the problem fast and gives you a clear mind to treat your design. Next, arrange time well. This project calls us to always improve our design of the CPU continuously. Sometimes the change we make to our design cost a lot of time. And all the parts of the design are mutual related, so there may be always some unexpected happens. Besides, each individual part of the CPU may be separately compiled correct does not mean that they can work together with control signals well. So the most important thing we keep in mind is that the design of the CPU project will never be perfect. And we need to always improve the design.

Also, we recommend students to try different methods of building the CPU such as single cycle, multi cycle and pipeline ways.